IN THE CLAIMS:

Please amend the claims as indicated below.

1. (Currently Amended) A method for reducing leakage current in a read only memory device, comprising the step of:

positioning a precharge phase prior to an evaluation phase during each read cycle of said read only memory device, wherein said precharge phase terminates independent of a clock edge.

2. (Original) The method of claim 1, further comprising the step of terminating said precharge phase by a clock edge.

3. (Original) The method of claim 2, wherein said precharge phase lasts for approximately one-half of said read cycle.

4. (Original) The method of claim 1, wherein said precharge phase is internally timed out prior to a subsequent clock edge.

5. (Original) The method of claim 4, wherein said precharge phase is less than one-half of said read cycle.

6. (Currently Amended) A read only memory device, comprising:

one or more transistors; and

a circuit to read said one or more transistors during a read cycle, wherein each read cycle positions a precharge phase prior to an evaluation phase, wherein said precharge phase terminates independent of a clock edge.

7. (Original) The read only memory device of claim 6, wherein said precharge phase is terminated by a clock edge.

8. (Original) The read only memory device of claim 7, wherein said precharge phase lasts for approximately one-half of said read cycle.

9. (Original) The read only memory device of claim 6, wherein said precharge phase is internally timed out prior to a subsequent clock edge.

10. (Original) The read only memory device of claim 9, wherein said precharge phase is less than one-half of said read cycle.

11. (Currently Amended) A method for reading a read only memory device, comprising the step of:

precharging said read only memory device during each given read cycle; and

evaluating said read only memory device following said precharging of said read only memory device during each given read cycle, wherein said precharge phase terminates independent of a clock edge.

12. (Original) The method of claim 11, further comprising the step of terminating said precharge phase by a clock edge.

13. (Original) The method of claim 12, wherein said precharge phase lasts for approximately one-half of said read cycle.

14. (Original) The method of claim 11, wherein said precharge phase is internally timed out prior to a subsequent clock edge.

15. (Original) The method of claim 14, wherein said precharge phase is less than one-half of said read cycle.

16. (Previously Presented) A method for reducing leakage current in a read only memory device, comprising the step of:

precharging at least one memory column in said read only memory device during a precharge phase of each read cycle, wherein at least one memory column is not precharged during a standby phase.

17. (Original) The method of claim 16, further comprising the step of terminating said precharge phase by a clock edge.

18. (Original) The method of claim 16, wherein said precharge phase is internally timed out prior to a subsequent clock edge.

19. (Previously Presented) A read only memory device comprised of memory columns that are connected to a precharge power supply during a precharge portion of each read cycle and are not connected to a precharge power supply during a standby mode.

20. (Original) The read only memory device of claim 19, wherein said read only memory device is further configured to terminate said precharge phase by a clock edge.

21. (Original) The read only memory device of claim 19, wherein said precharge phase is internally timed out prior to a subsequent clock edge.

22. (Currently Amended) An integrated circuit, comprising:

a read only memory device, comprising:

one or more transistors; and

a circuit to read said one or more transistors during a read cycle, wherein each read cycle positions a precharge phase prior to an evaluation phase, wherein said precharge phase terminates independent of a clock edge.

23. (Original) The integrated circuit of claim 22, wherein said precharge phase is terminated by a clock edge.

24. (Original) The integrated circuit of claim 23, wherein said precharge phase lasts for approximately one-half of said read cycle.

25. (Original) The integrated circuit of claim 22, wherein said precharge phase is internally timed out prior to a subsequent clock edge.

26. (Original) The integrated circuit of claim 25, wherein said precharge phase is less than one-half of said read cycle.